1 for AP

DOCKET NO. 04-SH-122 **PATENT**
CLIENT NO. STMI01-04122
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	Stuart Ryan, et al.
Serial No.	:	10/621,012
Filed	:	July 15, 2003
Title	:	PROTOTYPING INTEGRATED SYSTEMS
Art Unit No.	:	2185
Examiner	:	Denise Tran

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
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REPLY BRIEF

This Reply Brief is submitted on behalf of Appellant for the application identified above.

Please charge any additional necessary fees to Deposit Account No. 50-0208.

ARGUMENT

The rejection of claims 1–6, 8–9, 12–17 and 26 under 35 U.S.C. § 102(e).

As previously noted, independent claims 1, 12 and 26 all recite an interface and first and second address maps, where the first address map allocates a first range of addresses to an on-chip resource and a second range of addresses to an off-chip interface while the second address map allocates the first range of addresses to the off-chip interface. That is, the first range of addresses map to an on-chip resource in the *first address map* while that same first range of addresses map to the interface in the *second address map*; *only* the second range of addresses map to the interface in the *first address map*. The Examiner's answer asserts that the claims do not recite such a limitation:

> What the claims actually recite is "wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface."

Examiner's Answer at page 8. However, the Examiner does not explain how that language of the claim differs from the description of the claim limitation above. The claim language "wherein said first address map has a first range of addresses allocated to said at least one on-chip resource" recites that the first range of addresses map to an on-chip resource in the *first address map*. The claim language "in said second memory address map said first range of addresses are also allocated to the interface" – including the definite article "said" to indicate that the same first range of addresses as referred to previously within the claim – recites that the same first range of addresses map to the interface in the *second address map*. The claim language "wherein said first address map has a

second range of addresses allocated to said interface" recites that "*only* the second range of addresses map to the interface in the *first address map*." Addresses, by their nature, must each uniquely map only to a single memory location or resource, one address to one and only one memory location or resource. Otherwise, an address is useless and does not allow the system to access a particular memory location or resource. By reciting that a first range of addresses maps to an on-chip resource within a first address map, the claim intrinsically precludes said (the same) first range of addresses from mapping to anything else within the first address map. It is unclear, therefore, why the Examiner asserts that the claims do NOT recite the limitations as described. If the Examiner is asserting that "address" (or the plural "addresses" or "range or addresses") encompasses address(es) that can be simultaneously mapped to two or more memory locations and/or resources, such interpretation has not previously been clearly stated within the record, and Applicants have not been afforded a reasonable opportunity to address – no pun intended – a rejection based on such an interpretation.

The Examiner further asserts:

> Nothing in this claim limitation precludes additional ranges of addresses being mapped to the interface in the first address map.

Examiner's Answer at page 8. It is unclear how that statement is relevant to the issue to be decided. If an additional range of addresses – other than the first range of addresses – maps to the interface in the first address map, then those addresses fall within the recited second range of addresses within the address map. Regardless, such additional addresses are NOT part of the recited first range of

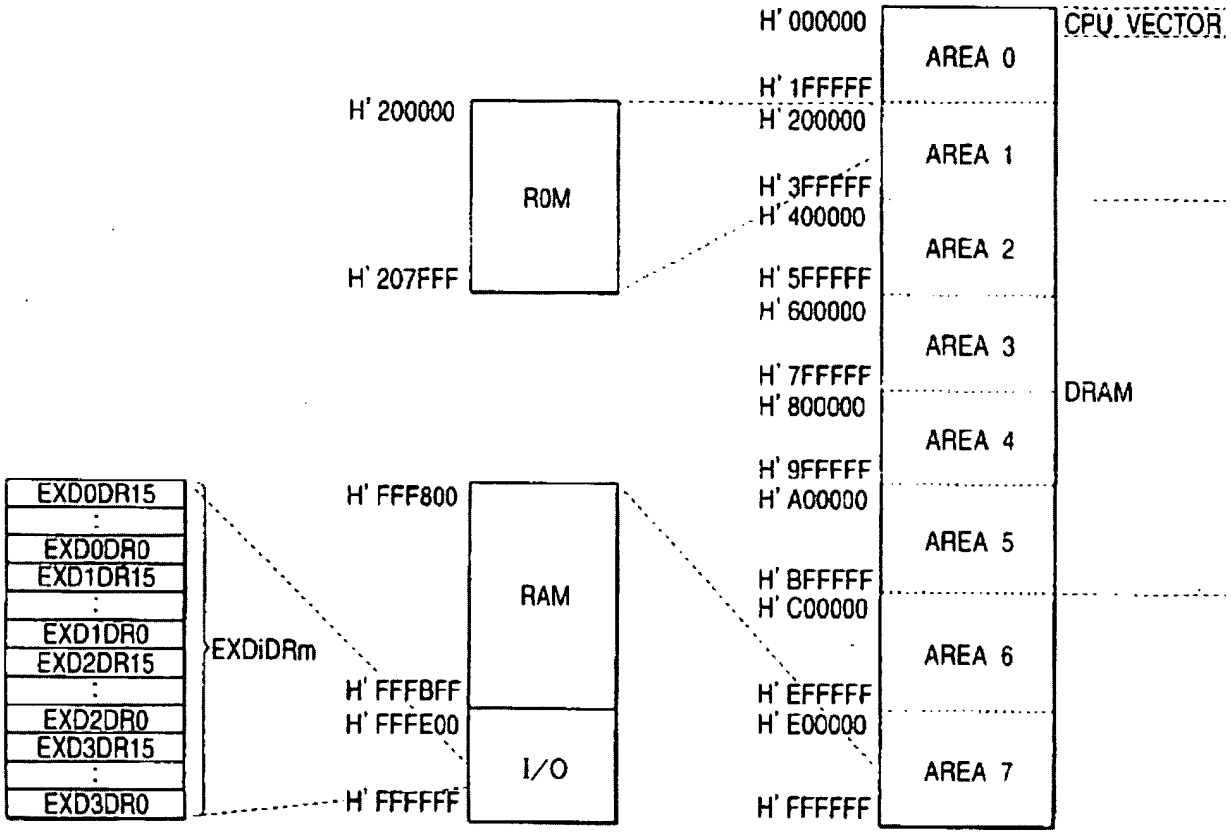
addresses, which are specified by the claim as mapping to an on-chip resource, not to the interface. Accordingly, the existence of additional addresses other than the first range of addresses is irrelevant to whether the limitation is satisfied by *Mituishi et al.*

The Examiner's Answer further states:

> Moreover, even if one were to assume that appellants overly narrow interpretation of this claim interpretation [sic] is correct, Mitsuishi also teaches the first range of addresses map to an on-chip resource in the first address map (e.g., fig. 2, area 7, address range H'E00000-H'FFFFFF [sic] map to an on chip RAM 6; fig. 1, RAM 6 and col. 14, lines 8-10) while that same first range of addresses map to the interface in the second address map (e.g., fig. 2, area 7, addresses range H'E00000-H'FFFFFF [sic] maps to an I/O interface (ports, means, registers) via an interface 12 including external bus controller 121 and EXMDAC 4 or maps to an external device via I/O means; fig. 1, controller 12, IOP and col. 14, lines 15-30, col. 17, line 60 to col. 18, line 15) . . .

Examiner's Answer at page 9. It is unclear what interpretation of the claims is being adopted by the Examiner for the purposes of this rejection, or how exactly the Examiner asserts that the claim limitation is satisfied. As an initial matter, the range of addresses "H'E000000-H'FFFFFF" is **NOT** disclosed by *Mitsuishi* as mapping to RAM as asserted by the Examiner. Instead only a portion of the address range H'E00000 to H'FFFFFF, (i.e., "Area 7"), corresponding to the subset of addresses H'FFF800 to H'FFFBFF, maps to RAM:

FIG. 2



Mitsuishi, Figure 2. Similarly only a portion of "Area 7" corresponding to the subset of addresses H'FFFE00 to H'FFFFFF maps to I/O. The Examiner seems to believe that the claim limitation "a first range of addresses allocated to said at least one on-chip resource" can encompass a range of addresses that is partially allocated to an on-chip resources (such as an on-chip RAM) and that the claim limitation "a second range of addresses allocated to said interface" similarly can encompass the same range of addresses if they are partially allocated to an interface. If so, however, such an

interpretation has not previously been clearly stated within the record (and indeed has not yet been explicitly stated), and Applicants have not been afforded a reasonable opportunity to address a rejection based on that interpretation. Moreover, an interpretation of "a . . . range of addresses allocated to" an on-chip resource and/or interface as meaning "*at least partially* allocated to" an on-chip resource and/or interface is unreasonable, unsupported by the specification or any evidence of record, and contrary to the ordinary meaning of the term "allocated" to those of ordinary skill in the relevant at, and is therefore arbitrary and capricious. That interpretation is also clearly adopted solely based on the results-oriented objective of contorting the claim to read on the cited reference.

The portion of the Examiner's Answer quoted above also seems to suggest that the Examiner believes that the claim limitation may be satisfied by a range of addresses allocated to an interface (for directing packets off-chip) such as a bus via which an on-chip resource may be selectively accessed. Again, such an interpretation has not previously been clearly stated in the record, and is not even now explicitly stated. Applicants have not had an opportunity to rebut such an interpretation prior to the close of prosecution. Moreover, such an interpretation is unreasonable, unsupported by the specification or any evidence of record, and contrary to the ordinary meaning of the term "allocated" to those of ordinary skill in the relevant art, and is therefore arbitrary and capricious. The interpretation is also clearly adopted solely based on the results-oriented objective of contorting the claim to read on the cited reference.

The Examiner's Answer asserts that Figure 2 of *Mitsuishi* shows multiple address maps, by

treating area 7 and areas 2-5 as separate address maps. Even if such an interpretation is true, the claim requires that both address maps have the same range of – that is, that both have the first range of addresses. Area 7 and areas 2-5 in *Mitsuishi* have different ranges of addresses.

REQUESTED RELIEF

The Board is respectfully requested to reverse the outstanding rejections and return this application to the Examiner for allowance.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Munck Butrus Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS CARTER, P.C.

Date: 2-11-2005

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